Active Thermal Control optimization and evaluation with detailed simulation and different lifetime models

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***Abstract* - Silicon carbide (SiC) power semiconductors are superior to traditional silicon devices due to their higher efficiency and performance, but face challenges related to temperature swings caused by very low thermal capacity, which limits their lifespan. To address this issue, this study proposes control methods to regulate the junction temperature of the SiC devices also referred to as Active Thermal Control (ATC). This approach reduces temperature swings, thereby extending the lifetime of SiC devices. The article examines the practical impact of thermal management implementation. Main goal is to present advantages from system perspective, that can be gained in terms of longer life expectancy by reducing thermal stresses. The benefits were evaluated with three different lifetime models using a high-resolution simulation with a small timestep, that allowed detailed observation of switching behavior and thermal transients at the transistor level. Across all tested models, even a basic temperature management algorithm, implemented without any hardware modifications, resulted in quantifiable improvements.**

Keywords - silicon carbide (SiC) inverter, active thermal control (ATC), remaining useful lifetime (RUL), lifetime prediction, power cycling, reliability

I. INTRODUCTION

The global adoption of electric vehicles (EVs) is on the rise, driven by environmental concerns and technological advancements. Power semiconductors are crucial to the operation of EVs, serving as key components in vital powertrain systems such as inverters, battery management systems, and chargers. Automakers are increasingly focusing on advanced technologies such as wide band gap devices like silicon carbide (SiC) and gallium nitride (GaN) with integrated drive topologies to enhance performance, lower mass, and reduce costs [1]. Along with striving to increase power density and reduce size, more significant thermal management problems may occur. The reduction in component size and thus smaller heat transfer area, negatively affects the heat dissipation capabilities. This results in higher junction temperatures, which can affect the lifespan of the power semiconductors [2]. Moreover, reducing size of the entire system, including heat sinks, decreases the total heat capacity – and thus significantly increases the temperature difference (ΔT_j) during a cycle. Continuous heating and cooling (thermal cycling) applies thermomechanical strain to the material layers [3].

Studies indicate that thermal cycling and resulting strains are primary factors in the accelerated deterioration which occurs due to frequent changes in the load current [4] and transistor switching. Because of the different thermal expansion coefficients of interfacing materials, failures commonly occur at the point of contact [5]. The most frequent thermally induced failure modes at the package level of semiconductor are bond wire lift-off and solder joint breakage [6], [7]. The vulnerability of these parts to failure due to thermal cycling necessitates a solution. One way of solving this problem is to actively control junction temperature during operation, which is the focus of this research and is referred to as active thermal control techniques (ATC). Studies on failure cycles and lifetime modeling suggest that large temperature swings reduce semiconductor lifespan more significantly than continuous operation at a higher mean junction temperature [8], [9]. Different active thermal control strategies are explored in the literature [10]. In general, we can divide these methods into two different approaches - manipulation of losses or heat dissipation. Many of these methods require additional hardware modifications, making implementation on existing systems complex and costly. Moreover, strategies like load current control and modulation coefficient control increase overall control complexity. Relatively simpler alternative - adjusting transistor switching frequency, has been suggested [11], [12], [13]. This method is inexpensive to implement, can be tested on existing inverters, and does not require any hardware changes. However, its effectiveness in mitigating temperature-induced failures, its impact on overall SiC inverter system performance and the optimization of ATC strategies, remain insufficiently explored.

Existing studies on ATC typically validate their approaches using only a single semiconductor lifetime model, which limits the ability to generalize conclusions. Since different lifetime models vary significantly due to differences in parameter conditions, device characteristics, and modeling approaches, relying on just one model may overlook key insights. Furthermore, prior research often focuses on the benefits of ATC without thoroughly analyzing its potential drawbacks, such

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as inverter current distortion caused by switching frequency adjustments. To address these gaps, this study evaluates ATC strategies across three different lifetime models, helping to identify mutual trends. Additionally, the high-resolution, short-timestep model enables a more comprehensive understanding of both benefits and possible trade-offs of ATC. Detailed approach facilitates implementation by enabling pre-optimization of crucial control parameters (e.g. switching frequency range).

First, an analytical modeling of semiconductor conduction and switching losses is presented in section II. It is followed by the description of junction temperature estimation and the active thermal control method used. Section III describes the lifetime model of the semiconductor and lifetime estimation with quantitative analysis using Rainflow method. Section IV presents results, sensitivity analysis for three lifetime models and achievable lifetime extensions with different control parameters and system optimization.

II. Loss Modelling, Junction Temperature Estimation and Active Thermal Control

Junction temperature measurement is crucial to ensure effective thermal management. This value can be obtained with direct methods or estimations. Direct methods, despite their high accuracy, have several drawbacks. For example, optical measurement requires an optical connection to the semiconductor, which prevents the use of common dielectric gel [14]. On the other hand, contact measurement introduces non-negligible delay. Utilizing a model-based approach, the thermal response time of the physical system and measurement circuits can be omitted, enabling predictive control behavior.

A. Loss Modelling

Effective thermal management of transistors is based on accurately estimating power losses during conduction and switching period. Conduction losses occur in both transistor and reverse diode. However, the majority of these losses is caused by the voltage drop on essential SiC transistor parameter - on-state drain source resistance R_{on}.

$$P_{\mathrm{c,M+D}} = \frac{1}{T_{\mathrm{sw}}}\int_0^{T_{sw}} \left[V_{\mathrm{fd}} i_f(t) + R_{\mathrm{fd}} i_f(t) + R_{\mathrm{on}} {i_d}^2(t)\right] dt \quad (1)$$

Average losses in three-phase two-level inverter per one period with SVPWM modulation can be calculated based on peak current (I_{m}), modulation coefficients (M), parallel conduction angle (β) and power factor ($\cos\varphi$). The general formula for conducting losses in single SiC transistor is [15]:

$$\begin{aligned} P_{c,T} = &\frac{R_{\mathrm{on}} I_{\mathrm{m}}^2}{4\pi}\cdot(AB+CD) \\ &+\frac{R_{\mathrm{on}} I_{\mathrm{m}}^2}{4\pi(R_{\mathrm{on}}+R_{\mathrm{fd}})^2}\cdot\Big(R_{\mathrm{fd}}^2 I_m^2\cdot(A\pi - B\pi - CD) \\ &+ V_{\mathrm{fd}}^2\big((\pi-2\beta)A - D\cos(\beta)\big) \\ &+ I_{\mathrm{m}}^2 R_{\mathrm{fd}} V_{\mathrm{fd}}(4A\cos(\beta) - D\pi + BD)\Big) \end{aligned} \quad (2)$$

where:

$$\begin{cases} A = 1 - 2t_{\mathrm{bl}} f_{\mathrm{sw}} \quad (3) & B = \dfrac{\pi}{2} + \beta - \dfrac{\sin(2\beta)}{2} \quad (4) \\ C = \cos(\beta) - \dfrac{\cos^2(\beta)}{3} \quad (5) & D = 2M\cos(\varphi) \quad (6) \end{cases}$$

Reverse diode conducts only in the situation where voltage drop on the SiC transistor will be higher than forward voltage of a diode:

$$\sin(\beta) = \frac{V_{\mathrm{fd}}}{R_{\mathrm{on}} I_{\mathrm{m}}} < 1 \quad (7)$$

Because of very high forward voltage, in most applications, reverse diode rarely conducts during operation, contributing negligibly to total losses. Therefore, β angle can be assumed as equal to $\frac{1}{2}\pi$ and conducting losses formula is simplified to:

$$P_{\mathrm{c}} = \frac{R_{\mathrm{on}} I_{\mathrm{m}}^2}{4} \quad (8)$$

Switching losses in transistors occur during transition between the on-state and off-state and can be significant in high-frequency power conversion systems. They are calculated by integrating the product of the current and voltage during the switching events [16]:

$$P_{\mathrm{sw}} = \left(\frac{1}{T_{\mathrm{on}}}\int_0^{T_{\mathrm{on}}} U_d(t) i_d(t) dt + \frac{1}{T_{\mathrm{off}}}\int_0^{T_{\mathrm{off}}} U_d(t) i_d(t) dt\right)\cdot f_{\mathrm{sw}} \quad (9)$$

A simpler approach to calculate average switching losses is by using data from the transistor's datasheet (E_{on}, E_{off}), typically given for specific voltage and temperature conditions. The most common method is to employ multi-dimensional lookup tables combined with linear approximation of the loss curve. Single cycle energy loss is then multiplied by the number of switching events, giving the switching power loss in one transistor. Since a single transistor does not conduct throughout the entire fundamental sinewave period and drain current i_d varies, average switching losses can be calculated based on half-wave equivalent DC current:

$$I_{\mathrm{DC}} = \frac{I_{\mathrm{m}}}{\pi} \quad (10)$$

$$P_{\mathrm{sw}} = f_{\mathrm{sw}}\cdot\left(E_{\mathrm{on(I_{DC},U,T)}} + E_{\mathrm{off(I_{DC},U,T)}}\right) \quad (11)$$

summing up, total estimated losses of three-phase inverter are:

$$P_{\mathrm{inv}} = (P_{\mathrm{c}} + P_{\mathrm{sw}})\cdot 6 \quad (12)$$

B. Junction Temperature Estimation

Accurate estimation of the semiconductors junction temperature is possible by utilizing the calculated power losses along with the thermal characteristics of the device - thermal resistance (R_{th}) and capacitance. These parameters are used to describe the heat flow from the junction to the ambience. Typically, junction to case ($R_{\mathrm{thj\text{-}c}}$) and case to ambient ($R_{\mathrm{thc\text{-}a}}$) thermal resistances are obtained from components datasheets. Then, the steady-state temperature of all power modules with common heatsink can be calculated as [17]:

$$T_{\mathrm{j}} = T_{\mathrm{amb}} + P_{\mathrm{inv}}\cdot\left(\frac{R_{\mathrm{thj-c}}}{6} + R_{\mathrm{thc-a}}\right) \quad (13)$$

C. Active Thermal Control

The chosen method of active thermal control performs its function by controlling the switching frequency of the transistors. By adjusting the switching frequency (f_{sw}), the switching losses (P_{sw}) can be controlled, leading to changes in junction temperature T_j (Fig. 1). Affecting total losses, this approach helps maintain a more stable junction temperature while reducing the number of large thermal cycles. The control algorithm aims to keep the estimated temperature at the same value as reference temperature value from the virtual heat sink. The core principle of the control system is to increase the switching frequency if the estimated temperature is lower than the reference temperature or decrease it when the estimated temperature rises. Implementing this control strategy reduces the number of cycles with extreme temperature difference, which are the primary contributors to transistor wear and lifespan reduction.

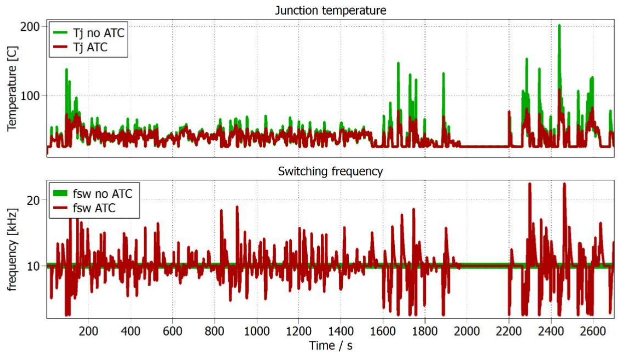

Fig. 1. Junction temperature comparison with ATC (red) and without ATC (green).

In this work, two temperature estimation signals can be distinguished. Both are calculated directly from the determined losses, multiplied by the thermal resistance. Thermal capacitance of the semiconductor can be modelled using Kalman or lowpass filter. Assuming a lower heat capacitance in the estimation than in the real object gives possibilities for predictive control and allows faster response to upcoming changes. With this approach, the estimated signal anticipates temperature changes before they actually occur, enabling the control system to react in advance. The second signal is a reference signal, additionally passed through another Kalman filter with a lower response speed. The filter emulates a virtual heat sink [3] with a higher heat capacity, which averages the temperature over a time interval (Fig. 2).

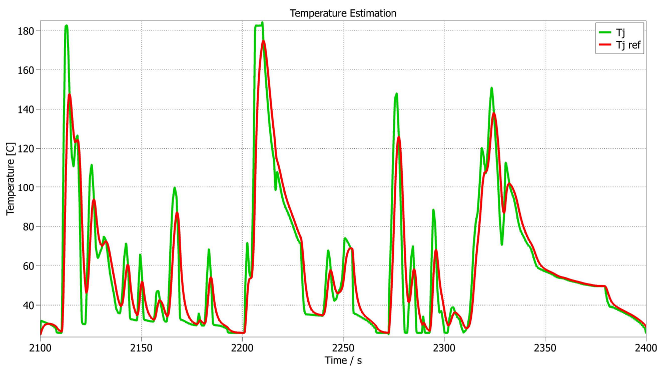

Fig. 2. Estimated temperature - no heat capacitance (green) and reference temperature with virtual heat sink capacitance (red).

For purposes of this study, only proportional controller with dead zone was implemented. Such a solution has quite a few advantages. Damping rapid changes in the response is achieved through a low-pass filter or a Kalman filter. Dead zone implementation reduces unnecessary small output changes, additionally improving stability (Fig. 3).

The use of only the proportional component in the controller ensures that the output is maintained at the same level for the same difference between T_j and $T_{j,ref}$, without the influence of the previous state. This approach keeps the average switching frequency close to a predefined nominal level, which is crucial for maintaining overall system performance. Decreasing average switching frequency can negatively affect the integrated drive system by increasing total harmonic distortion (THD) of the current generated by the inverter [18], which leads to torque ripple [19] and increased machine losses [20]. Conversely, higher switching frequency causes higher switching losses and higher copper losses caused by skin effect.

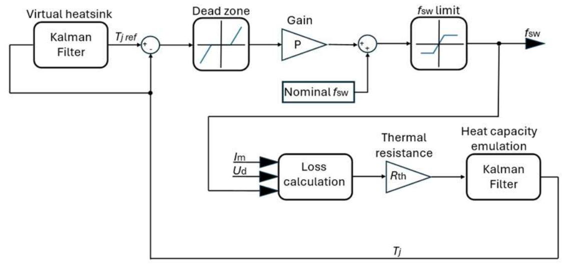

Fig. 3. ATC control schematic.

Two approaches for this ATC technique can be distinguished:

Method A sets a nominal frequency in the middle of the possible control range (or at the point of highest efficiency). In this case, the frequency can both decrease and increase during transients.

Method B sets the base switching frequency as the maximum nominal one for the system. The frequency can be only reduced when the estimated temperature increases, returning to the initial state after a certain period. Application with method B cannot respond to a decrease in temperature once a steady state at high temperature is reached. In this case, increasing the switching frequency above the nominal value to reduce the temperature change slope is not possible. The plot of frequency changes for both methods is shown in Fig. 4.

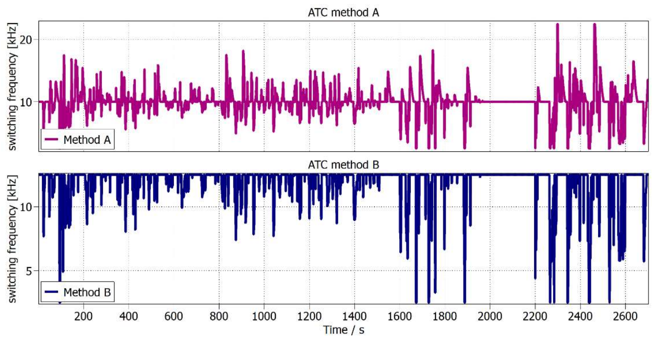

Fig. 4. Two methods of adjusting the switching frequency in ATC.

III. LIFETIME ESTIMATION

In order to evaluate the benefits of active control, methodology with remaining useful lifetime (RUL) models were used. Temperature changes are calculated based on transistor losses during example drive cycle. Then, quantitative analysis (Rainflow method) is performed on the temperature graph [21]. RUL models estimate the time to failure (in number of cycles) as a function of temperature swings (Fig. 5).

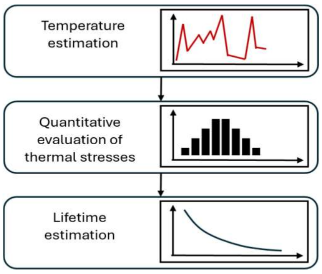

Fig. 5. Lifetime evaluation methodology.

A. Lifetime model

The most fundamental determinant of a semiconductor's lifetime is the relationship between the number of cycles to failure and thermal cycling amplitude. As thermal cycling in the real operating conditions is irregular and varies in magnitude, it is not possible to determine the lifetime curve of a semiconductor directly from it. To estimate the expected lifetime more predictably, accelerated lifetime tests - have been developed (e.g. HTGB [22], H3TRB [23], PC [24]). With these tests, carried out under uniform, stable conditions, it is possible to make an approximate estimation of the lifetime of a semiconductor during operation time. Using data from accelerated lifetime tests, semiconductor suppliers can derive empirical formulas to predict the number of cycles to failure.

General overview of the lifetime of a transistor can be obtained using commonly available models. Since the ATC method primarily aims to reduce high-amplitude thermal cycles, leading to an inevitable increase in low-amplitude cycles, it is essential to use a transistor lifetime model that is particularly accurate for small temperature swings. In this work, the primary model used is the one proposed by F. Hoffmann, S. Schmitt and N. Kaminski in [25], referred as EPE20 model.

Lifetime model formula includes several material constants β_1, β_2, θ_1, θ_2, K (Table I) and $T_{\min}$ – ambient temperature, with N_f representing the number of cycles to failure (Fig. 6).

$$N_{\mathrm{f}} = K \cdot (\Delta T_{\mathrm{j}})^{\beta_1'} \cdot e^{\left(\frac{\beta_2}{T_{\min}}\right)} \tag{14}$$

Where β_1' is:

$$\beta_1' = e^{-\left(\frac{\Delta T_{\mathrm{j}} - \theta_1}{\theta_2}\right)} + \beta_1 \tag{15}$$

TABLE I. FITTING PARAMETERS OF EPE20 LIFETIME MODEL

β_1	β_2	θ_1	θ_2	K
-3.581	1537	26	13	1.31×10^{10}

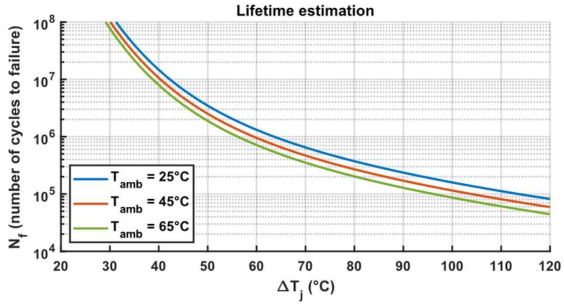

Fig. 6. Lifetime plot of semiconductor vs amplitude of temperature swing for different ambient temperatures.

B. Rainflow analysis

The temperature diagrams from the simulation test allow for an approximate determination of the thermal stresses during the cycle. In this purpose - the Rainflow algorithm can be used. The algorithm returns the number of amplitudes Rc_i within a predefined amplitude range (Fig. 7). Next, the percentage of usage for a given number of cycles $N_f(\Delta T_j)$ can be determined (Fig. 8), relative to the test conditions (Fig. 6). Fig. 7 shows that with ATC applied, high-amplitude cycles are almost completely reduced, while the spectrum of amplitudes is shifted toward smaller values. As shown in Fig. 8, the contribution of low temperature swings to thermal degradation is relatively insignificant. The largest contribution to semiconductor usage is made by large temperature peaks. Although there are relatively few, they cause the greatest wear of the semiconductor.

The next step is to sum up the damage for each magnitude range. The result is the percentage wear of the semiconductor during the test run. Using the proportional inverse of the percentage wear over the test duration t_{TD}, the estimated time to failure (TTF) in operating hours (or vehicle range) can be calculated:

$$TTF = \frac{t_{\mathrm{TD}}}{\sum_i \frac{Rc_i}{N_{\mathrm{f}}\left(\Delta T_{\mathrm{j}_i}\right)}} \tag{16}$$

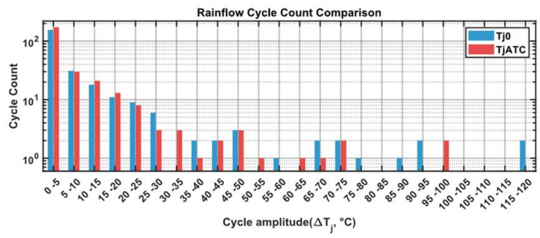

Fig. 7. Rainflow analysis for a test drive with ATC (red) and without (blue).

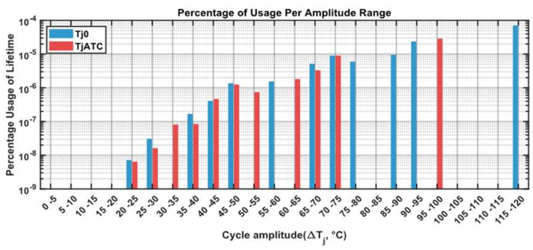

Fig. 8. Percentage of expected semiconductor usage per amplitude range.

IV. Simulation results analysis

Buses and trucks are commercial vehicles with high utilization, often operating 16–24 hours per day, making them more vulnerable to semiconductor wear. Therefore, simulations were performed with an example driving cycle for a heavy-duty diesel truck. Based on the cycle and the vehicle's motion equations, the required speed and external torque at a given time are modeled. This determines the voltage and current of the inverter. Semiconductor losses, and then temperature, are calculated based on the inverter's currents and voltages (Fig. 9). The parameters of the modelled vehicle are listed in Table II and the power module parameters are listed in Table III.

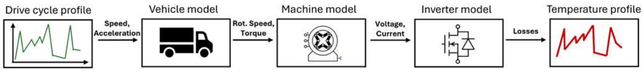

Fig. 9. Simulation setup.

Table II. Vehicle parameters

Drag coeff. [-]	Front area [m²]	Mass [kg]	Wheel radius [m]	Gear ratio [-]
0.53	9.7	40000	0.5	19

Table III. Power module parameters

Ron [mΩ]	Rth [°C/W]	Eon [mJ]	Eoff [mJ]
3.0	0.118	0.0926 × i(t)	0.0388 × i(t)

A. Switching range influence

The frequency range is a key parameter in ATC control. Frequency adjustments are typically made within a range defined by the physical limitations of the inverter. The lower frequency limit is set by the maximum total harmonic distortion (THD) allowed in the current supplied to the machine. The upper limit is usually constrained by junction temperature limits, increased electromagnetic interference (EMI), or insulation exposure. In most EV applications, a 10 kHz switching frequency is considered standard and serves as a nominal baseline. In this study, all frequency range adjustments were made relative to this reference point. In Tables IV and V, both active thermal control switching frequency strategies are compared to the reference application without ATC. To ensure a fair evaluation of these methods and the reference case, the comparison was made for the same average switching frequency. This way, the average switching losses and other frequency dependent losses are also similar.

Table IV. Lifetime estimation with method A compared to refence application (without active thermal control)

Method A					no ATC (for the same average f_{sw})	
Swtching range [kHz]		*average f_{sw} [kHz]*	*lifetime [10^3 km]*	*Average T_j [°C]*	*lifetime [10^3 km]*	*Average T_j [°C]*
Low	*High*					
8	12	9.9	567	58.5	329	58.8
6	14	9.9	864	58.3	329	58.8
4	16	9.8	949	58.2	340	58.7
2	18	9.8	950	58.1	340	58.7
2	24	9.8	950	58.1	340	58.7

Table V. Lifetime estimation with method B compared to refence application (without active thermal control)

Method B					no ATC (for the same average f_{sw})	
Swtching range [kHz]		*average f_{sw} [kHz]*	*lifetime [10^3 km]*	*Average T_j [°C]*	*lifetime [10^3 km]*	*Average T_j [°C]*
Low	*High*					
2	10	9.7	949	58.1	341	58.3
2	14	13.3	326	62.2	142	62.8
2	18	17.2	149	66.5	61	67.3
2	22	21.1	76	70.9	30	71.8

Both method A and method B can improve transistor lifetime compared to a system without any form of thermal control. Method A performs better with an increase in switching frequency range - as the control system has bigger capabilities. On the other hand, method B experiences a significant decrease in lifetime as the switching frequency range increases. This decline occurs because, in method B, the nominal switching frequency is always set to the maximum frequency. Shifting maximum frequency towards higher values, increases average losses and average temperature, ultimately reducing the device's lifetime. Therefore, these two methods cannot be directly compared over wider frequency control range. Method A is more adaptive, as it allows both an increase and decrease in switching frequency. This means it can respond more effectively to both rising and falling temperatures, improving system thermal stability across various operating conditions. Additionally, by centering the frequency at an optimal efficiency point, Method A achieves a better balance between overall losses and power cycling control performance across a broader range of operating conditions. However, beyond a certain point (4-16 kHz for the test case), further increases in the frequency range no longer provide any lifetime benefit. In fact, they may negatively impact the drive system by increasing switching losses and EMI. Therefore, in the following study, Method A was chosen as the more comprehensive approach, with a switching range of 4–16 kHz identified as optimal.

B. Estimated lifetime comparison with different lifetime models

A comparative analysis was conducted on three different semiconductor lifetime prediction models to assess the sensitivity of lifetime estimation results. In addition to the EPE20 model described earlier, CIPS08 [4] and SKiM63/93 [26] models were tested. The CIPS08 model is similar to the EPE20 model used in the previous analysis, as it employs the same formula (14), but it is not calibrated for low-temperature swings. The parameters for the EPE20 model are provided in Table I (Section III.A), while the parameters for the CIPS08 and SKiM63/93 models are listed in Tables VI and VII below.

Table VI. Fitting parameters of CIPS08 lifetime model

β_1	β_2	θ_1	θ_2	K
-3.581	1537	n/a (0)	n/a (0)	1.31×10^{10}

Table VII. Fitting parameters of SKiM63/93 lifetime model

β_1	β_2	θ_1	θ_2	K
-4.923	766	n/a (0)	n/a (0)	2.5×10^{13}

Lifetime estimations were conducted for the same temperature profile as in Table IV, incorporating method A. Results are presented in Fig. 10 and compared to the reference case (with no ATC implemented) for the same lifetime model.

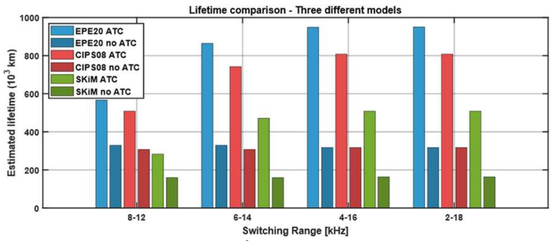

Fig. 10. Lifetime estimation (in 10^3 km) for different semiconductor models.

The three models produce significantly different results. Estimated lifetimes vary by up to a factor of two between models. Since lifespan depends on numerous factors, it is difficult to determine which model is the most accurate. The small difference between the EPE20 and CIPS08 models highlights how the model accuracy for small temperature swings affects the total estimated life expectancy. However, every model shows that implementing active temperature control extends the life of the semiconductor. All models, despite different coefficients and different estimated lifetimes, show very similar trends - implementation of ATC with a switching range of 8-12 kHz results in an increase in estimated lifetimes of about 50%, while for a switching range of 2-18 kHz there is an increase of up to 300%. These substantial improvements stem from the algorithm's emphasis on minimizing thermal cycle amplitudes, which form the sole basis for lifetime estimation in this study.

C. *Temperature control range influence*

Another important factor to consider when implementing ATC is the operating temperature range of active thermal control. For example, moving the ATC activation limit above 60°C, minimizes unnecessary frequency changes in a range that has little impact on transistor wear. Fig. 11 summarizes the test results for various ATC temperature active ranges, evaluated using the three models presented earlier. The results are expressed in relative lifetime value, compared to a reference case with ATC active in whole temperature range. In these tests, frequency adjustments were made using Method A, within a range of 4 to 16 kHz.

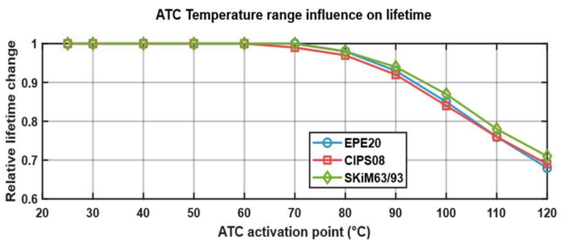

Fig. 11. Lifetime estimation for different temperature ranges (in relative values to the reference case with ATC active for whole temperature range).

Limiting excessive frequency changes at lower temperatures does not provide any significant benefit in terms of extending transistor lifespan. However, it does not have a negative impact up to approximately 70°C. Raising this limit further makes the algorithm less responsive to certain temperature spikes, ultimately reducing lifespan. This trend is consistent across all tested models. Despite this, reducing the numbers of less important frequency adjustments saves microcontroller computing resources and simplifies control system tuning by restricting its operation to a narrower temperature range. These benefits are enough to consider implementing a fixed temperature range.

D. *System level impact of ATC*

When introducing new functionalities, it is essential to consider potential drawbacks. In the case of ATC implementation, two main concerns arise. First, reducing the switching frequency below the nominal value may lead to increased THD. Second, frequency increase causes higher switching losses, which raise the actual semiconductor temperature. Fig. 12 illustrates the acceleration of the vehicle model. During the first two seconds, the phase current rises rapidly. In response to the significant increase in estimated temperature, the control system lowers the switching frequency to its minimum value (4 kHz). As a result, the initial temperature cycle reaches an amplitude of 110°C instead of 150°C. After a short time, the switching frequency gradually returns to its nominal value. Additionally, the temporary increase in switching frequency following the drop in current causes a temperature rise, which subsequently reduces the amplitude of the second cycle.

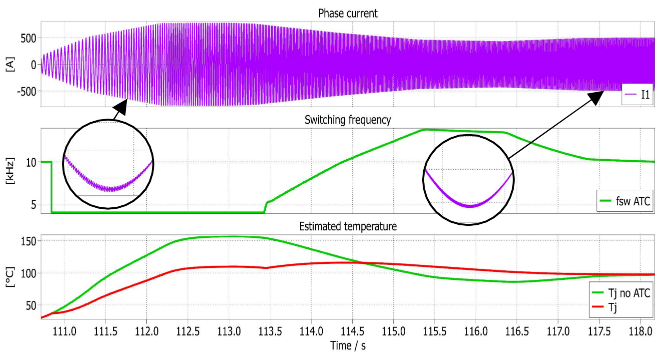

Fig. 12. Acceleration of the vehicle model – current, switching frequency adjustment and junction temperature during transient state.

A THD analysis was performed to assess the impact of frequency change during the transient illustrated in Fig. 12. In the worst-case scenario (f_{sw} = 4 kHz), the current THD reaches 4.4%, whereas at the nominal switching frequency of 10 kHz, it is 1.4%. The THD content, while strongly dependent on switching frequency, is also influenced by the current magnitude. Since the ATC algorithm typically reduces frequency during high current conditions (when temperature rises), the relative impact of increased current ripple is partially mitigated - helping to maintain THD within acceptable limits, even at lower switching frequencies. A preliminary analysis suggests that, from the inverter's THD perspective, the drawbacks of ATC are minimal and should not hinder adoption. However, operating at lower switching frequencies increases harmonic content in the motor's magnetic circuit, potentially leading to higher iron losses and increased thermal stress in the machine. Additionally, varying the switching frequency may raise concerns related to EMI and electromagnetic compatibility (EMC). As a result, ATC can shift the drive system away from its optimal efficiency point, as most systems are designed for operation at a fixed frequency.

V. Conclusion

Accelerated wear of the SiC semiconductors resulting from intensive thermal cycling is a non-negligible phenomenon but can be minimized at the converter control system design stage. For the three tested semiconductor lifetime models, the estimated operating time values can vary widely, but the scale of the benefits obtained by implementing ATC remains consistent. An optimized ATC strategy, through tuning frequency range and temperature thresholds, can extend lifetime by up to three times compared to systems without thermal control. This study shows that even a pure software change, requiring no hardware changes, no additional sensors, can effectively extend semiconductor lifespan. It is important to recognize that the presented lifetime estimates account only for thermal stress. Other factors, such as mechanical, electrical, or humidity-induced stress, which can significantly impact overall semiconductor lifetime, were not considered.

In this study, only the temperature of the power module was analyzed, while the motor was modeled purely from an electrical perspective, with thermal effects neglected. A comprehensive investigation of the impact of frequent switching frequency changes on the entire drive system, including both the inverter and the electrical machine, is planned for future work. Experimental validation is also planned, comparing the proposed algorithm implemented in two ways: the software-based frequency adjustment described in this paper, and an alternative hardware-based approach using gate resistance adjustment.

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